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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/001,594	10/31/2001	David J.C. Johnson	10013444 -1	1931

7590 07/26/2004

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P. O. Box 272400
Fort Collins, CO 80527-2400

EXAMINER

CHACE, CHRISTIAN

ART UNIT	PAPER NUMBER
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2187

DATE MAILED: 07/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/001,594	Applicant(s) JOHNSON ET AL.	
	Examiner Christian P. Chace	Art Unit 2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 June 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 October 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

This Office action has been issued in response to amendment filed 10 June 2004. Claims 1-10 are pending. Applicants' arguments have been carefully and respectfully considered in light of the instant amendment, but they are not persuasive. Accordingly, this action has been made FINAL, as necessitated by amendment.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Cheng et al (US Patent 5,655,103).

With respect to independent claim 1, a cache memory system is disclosed in figure 1, #101, for example, which shows a CPU and cache.

Storage for a plurality of data values is disclosed in figure 3 as an address, inclusion, and cross-interrogation bits, which are, of course, "data values." In addition, a cache, as shown in figure 1 #101, is a storage for a plurality of data values.

Storage for a plurality of "age bits," each age bit corresponding to one of the data values is disclosed in figure 3 as the "stale bit."

Each age bit indicating whether the corresponding data value is stale, has not been recently accessed, is disclosed in figure 3 as the “stale bit.” The stale bit is also discussed in the abstract, for example.

The stale bit is the age bit, and it shows that data has or has not been recently accessed, with “recently accessed” being the predetermined time period. Indicating that the age bit is stale when the age bit has remained at a particular logical state (stale bit set to zero) of at least a “predetermined time period,” is disclosed in the abstract as “[i]f the processor further modifies the cache line.” In other words, the time it takes the processor to further modify the cache line is the “predetermined time period.”

With respect to claim 2, each age bit indicating that the corresponding data value is stale is, again, disclosed in figure 3 and the abstract, as discussed supra.

Indicating that the age bit is stale, or has not been recently accessed, when the age bit has remained at a particular logical state (stale bit set to zero) of at least a “predetermined time period,” is disclosed in the abstract as “[i]f the processor further modifies the cache line.” In other words, the time it takes the processor to further modify the cache line is the “predetermined time period.”

With respect to claims 3 and 6, a state machine is disclosed in column 2, lines 31-32 as the memory controller.

The state machine “periodically” (see discussion of “predetermined time period” supra with respect to claim 2) determining the state of each age bit is discussed in the abstract as “setting the age bit.”

For each age bit that is not at the particular logical state, setting the age bit to the particular logical state is disclosed in the abstract, as discussed supra with respect to claim 1, and is also disclosed in column 2, lines 31-32 as "setting the stale bit."

With respect to claim 4, each age bit further indicating whether the corresponding data value is modified is disclosed in the abstract as, "If the first processor further modifies the cache line...the stale bit is set to one." In other words, the stale bit set to one indicates the data is modified, as well as stale.

With respect to claim 5, each age bit indicating that the corresponding data value is modified and has not been recently accessed is disclosed in the abstract as, "If the first processor further modifies the cache line...the stale bit is set to one." In other words, the stale bit set to one indicates the data is modified, as well as stale.

Doing so when the age bit has remained at a particular logical state for at least a predetermined time period is disclosed in the abstract as "[i]f the processor further modifies the cache line." In other words, the time it takes the processor to further modify the cache line is the "predetermined time period."

With respect to independent claim 7, a method of indicating whether an entry in a cache memory is stale, or has been recently accessed, is disclosed in the abstract.

Setting a bit to a first logical state when the entry is "accessed," is disclosed in the abstract as setting the stale bit equal to zero. "Accessing" is a load/miss request from a processor. Column 1, lines 17-21 and lines 27-28 discuss load/miss supplying (accessing) data to the CPU/[cache] (shown as one unit in figure 1, #101, for example.)

Setting the bit to a second logical state is disclosed in the abstract as setting the stale bit to one.

Determining that the entry is stale, or has not been recently accessed, when the bit is at the second logical state after at least a “predetermined time” after being set to the second logical state is disclosed in the abstract as “[i]f the processor further modifies the cache line.” In other words, the time it takes the processor to further modify the cache line (thereby setting the stale bit to the second logical state, or one) is the “predetermined time period.”

Indicating that the age bit is stale when the age bit has remained at a particular logical state (stale bit set to zero) of at least a “predetermined time period,” is disclosed in the abstract as “[i]f the processor further modifies the cache line.” In other words, the time it takes the processor to further modify the cache line is the “predetermined time period.”

With respect to independent claim 8, a method of detecting whether an entry in a cache memory is stale, or has been recently accessed, and dirty is disclosed in the abstract.

Setting a bit to a first logical state when the entry is “written,” is disclosed in the abstract as setting the stale bit equal to zero. “Writing” is a load/miss request from a processor. Column 1, lines 17-21 and lines 27-28 discuss load/miss supplying (writing) data to the CPU/[cache] (shown as one unit in figure 1, #101, for example.)

Setting the bit to a second logical state is disclosed in the abstract as setting the stale bit to one.

Determining that the entry is stale and dirty (modified) when the bit is at the second logical state after at least a “predetermined time” after being set to the second logical state is disclosed in the abstract as “[i]f the processor further modifies the cache line.” In other words, the time it takes the processor to further modify the cache line (thereby setting the stale bit to the second logical state, or one) is the “predetermined time period.”

“If the first processor further modifies the cache line...the stale bit is set to one.” In other words, the stale bit set to one indicates the data is modified, as well as stale.

Indicating that the age bit is stale when the age bit has remained at a particular logical state (stale bit set to zero) of at least a “predetermined time period,” is disclosed in the abstract as “[i]f the processor further modifies the cache line.” In other words, the time it takes the processor to further modify the cache line is the “predetermined time period.”

With respect to independent claim 9, a method of detecting whether at least one entry in a set of entries in a cache memory is stale, or recently accessed, is disclosed in the abstract.

Setting a bit to a first logical state when the entry corresponding to an index is “accessed,” is disclosed in the abstract as setting the stale bit equal to zero. The “index” is the dependency table shown in figure 3. As discussed with respect to independent claim 1, the index holds a “stale bit” value, which is the instantly claimed “bit.” “Accessing” is a load/miss request from a processor. Column 1, lines 17-21 and

lines 27-28 discuss load/miss supplying (accessing) data to the CPU/[cache] (shown as one unit in figure 1, #101, for example.)

Setting the bit to a second logical state is disclosed in the abstract as setting the stale bit to one.

Determining that at least one entry in the corresponding index is stale when the bit is at the second logical state after at least a “predetermined time” after being set to the second logical state is disclosed in the abstract as “[i]f the processor further modifies the cache line.” In other words, the time it takes the processor to further modify the cache line (thereby setting the stale bit to the second logical state, or one) is the “predetermined time period.”

Indicating that the age bit is stale when the age bit has remained at a particular logical state (stale bit set to zero) of at least a “predetermined time period,” is disclosed in the abstract as “[i]f the processor further modifies the cache line.” In other words, the time it takes the processor to further modify the cache line is the “predetermined time period.”

With respect to independent claim 10, a method of detecting whether at least one entry in a cache memory is stale, or recently accessed, and dirty is disclosed in the abstract.

Setting a bit to a first logical state when an entry “corresponding to an index” is modified is disclosed in the abstract as setting the stale bit equal to zero. The “index” is the dependency table shown in figure 3. As discussed with respect to independent claim 1, the index holds a “stale bit” value, which is the instantly claimed “bit.”

Setting the bit to a second logical state is disclosed in the abstract as setting the stale bit to one.

Determining that the entry is stale and dirty (modified) when the bit is at the second logical state after at least a “predetermined time” after being set to the second logical state is disclosed in the abstract as “[i]f the processor further modifies the cache line.” In other words, the time it takes the processor to further modify the cache line (thereby setting the stale bit to the second logical state, or one) is the “predetermined time period.”

“If the first processor further modifies the cache line...the stale bit is set to one.” In other words, the stale bit set to one indicates the data is modified (dirty), as well as stale.

Indicating that the age bit is stale when the age bit has remained at a particular logical state (stale bit set to zero) of at least a “predetermined time period,” is disclosed in the abstract as “[i]f the processor further modifies the cache line.” In other words, the time it takes the processor to further modify the cache line is the “predetermined time period.”

Response to Arguments

With respect to applicants’ argument that there are two common uses for the word “stale,” examiner respectfully disagrees. Applicants note that the first meaning is that the stale data has not been used recently. Applicants then offer what they allege to be a second definition of data being obsolete. Examiner notes that data that has not been used “recently” is, indeed, “obsolete.” This is the whole point for the use of age

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bits in the first place. This is a result of the temporal locality of reference phenomenon. For example, we use age bits in a system to tell us when data has been untouched for a period of time that, by percentage, usually means it is obsolete. If a data word has remained in a cache for a long time, chances are it is no longer the most up to date version of that data. It is also holding up space in the cache that could be used for other words that are being referenced much more often, thereby increasing the efficiency of the system. This is what Cheng et al are doing, and this is what applicants are doing.

With respect to applicants' argument that claim 1 specifies a cache memory, examiner wishes to clarify – claim 1 recites a “cache memory system,” which may include a cache memory. Applicants then argue that Cheng et al's stale bits are in a memory controller, not a cache memory. Regardless of whether or not this is accurate, it is not commensurate with the language of the claim. Claim 1 does not require the stale bits to be in a cache – it merely requires them to be in a cache memory system, which may include a controller, as applicants' cache memory system merely comprises the stated limitations. Therefore, the claim language is “open-ended,” if you will, and may include anything else in addition to the limitations.

With respect to applicants' argument that claim 1 specifies that each age bit is in the same structure as the corresponding data, examiner again, respectfully disagrees, and finds this argument is not commensurate with the claim language. The only structure required by the claim language is that of the cache memory system, the scope of which is discussed supra.

With respect to applicants' argument that claim 1 specifies that the age bits indicate whether corresponding data has been recently accessed, examiner agrees. However, examiner respectfully disagrees that Cheng et al do not show this limitation. As discussed supra with respect to the independent claims, indicating that the age bit is stale, or has not been accessed, when the age bit has remained at a particular logical state (stale bit set to zero) of at least a "predetermined time period," is disclosed in the abstract as "[i]f the processor further modifies the cache line." In other words, the time it takes the processor to further modify the cache line is the "predetermined time period." The bit shows whether the process has accessed the data within the "predetermined time period."

With respect to applicants' argument that claim 7 specifies setting a bit to a first logical state when the entry is accessed, examiner agrees. However, examiner respectfully disagrees that Cheng et al do not show this limitation. Applicants note that access can occur without a miss. This is true, but as applicants have merely claimed an "access," and nothing more particular, the "miss" of Cheng et al reads on the claim language as it stands. Also, the abstract states that "If the first processor further modifies the cache line.....the stale bit is set to one."

With respect to applicants' argument that claim 7 specifies determining an entry has not been recently accessed when the bit is at the second logical state for at least a predetermined time and that Cheng et al do not show this, examiner respectfully disagrees, and refers applicants to the independent claim rejections supra as well as the discussion fo this point in this section supra with respect to claim 1's arguments.

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With respect to applicants' argument with respect to claim 8 that writing can occur without a miss, examiner agrees, but respectfully points out again, similar to the discussion supra, such as, as applicants have merely claimed a "write," and nothing more particular, the "miss" of Cheng et al reads on the claim language as it stands. Also, the abstract states that "If the first processor further modifies the cache line....the stale bit is set to one."

With respect to applicants' argument that Cheng et al do not show the stale bits to indicate whether corresponding data has not been recently accessed, examine refers applicants to discussion of same supra.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).


A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

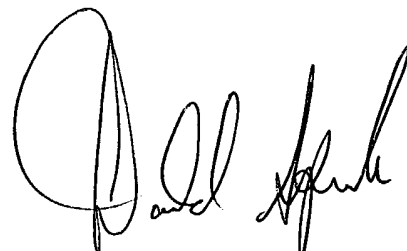
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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christian P. Chace whose telephone number is 703.306.5903. The examiner can normally be reached on 9-4-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 703.308.1756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Christian P. Chace 
DS/cpc


DONALD SPARKS
SUPERVISORY PATENT EXAMINER